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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,467	02/26/2004	Kristopher Craig Whitney	ROC920030309US1	7026

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EXAMINER	
MEHRMANESH, ELMIRA	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/787,467	WHITNEY, KRISTOPHER CRAIG	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on January 30, 2007 for the application of Whitney, for a "Method for achieving higher availability of computer PCI adapters" filed February 26, 2004.

Claims 4-19 are pending in the application.

Claim 18 has been amended.

Claims 1-3 have been cancelled.

Claim 19 has been added.

Claims 4, 7-8, 11, 18 are rejected under 35 USC § 102.

Claims 5-6, 9-10, 12-17, 19 are rejected under 35 USC § 103.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 4, 7-8, 11, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Emerson et al. (U.S. Patent No. 6,173,341).

As per claim 4, Emerson discloses a method for fault recovery in a computer system having a system processor (Fig. 2, element 102), an input/output processor (Fig. 2, element 210), and an input/output adaptor (Fig. 2, element 114) connected to the system processor and the input/output processor (Fig. 2) the input/output adaptor being configured to be dynamically switchable between being controlled by the system processor and being controlled by the input/output processor (col. 8, lines 30-54) the method for fault recovery comprising:

detecting a fault in the input/output processor and switching the input/output adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected (col. 8, lines 30-54).

As per claim 7, Emerson discloses the computer system has a plurality of dynamically switchable input/output adapters (Fig. 2, element 114) and each of the dynamically switchable input/output adapters being controlled by the input/output

processor (Fig. 2, element 210) when the fault is detected is switched to control by the system processor (col. 8, lines 30-54).

As per claim 8, Emerson discloses detecting correction of the fault in the input/output processor (Fig. 2, element 210) switching the input/output adapter to control by the input/output processor when the correction of the default is detected, if it was previously switched to control by the system processor as a result of the fault in the input/output processor (col. 8, lines 30-54).

As per claim 11, Emerson discloses the computer system has a plurality of dynamically switchable input/output adapters (Fig. 2, element 114) and each of the dynamically switchable input/output adapters being controlled by the system processor (Fig. 2, element 102) when the correction of the fault is detected is switched to control by the input/output processor if it was previously switched to control by the system processor as a result of the fault in the input/output processor (col. 8, lines 30-54).

As per claim 18, Emerson discloses the input/output adapter; the input/output processor and the system processor are interconnected via a bus (Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5-6, 9-10, 12-17, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson et al. (U.S. Patent No. 6,173,341) in view of Odenwald et al. (U.S. Patent No. 6,223,240).

As per claims 5, 9, and 16 Emerson fails to explicitly disclose a PCI adaptor.

Odenwald teaches:

the input/output adapter is a PCI (Peripheral Component Interconnect) adapter (Fig. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of configuring adapters in a computer system of Emerson et al.'s in combination with the method of sharing processing load among a plurality of devices of Odenwald et al.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Emerson et al. discloses a method of assigning input/output adapters to input/output processors and host system processors (Figs. 2 and 4). Emerson discloses using a downloadable drive module to address the problem of I/O bottlenecks (col. 3, lines 14-21).

Emerson discloses an efficient method and system for assigning and controlling in an I_2O environment (col. 9, lines 23-34), which is capable of additional rearrangements, modifications and substitutions (col. 9, lines 46-50).

Odenwald et al. discloses a method of using a bus bridge to connect input/output adapters and processors to the host processor to provide an improved method for input/output transaction processing (col. 9, lines 9-20), which is considered a modifications/substitutions of Emerson's system.

As per claims 6, 10, and 17 Emerson fails to explicitly disclose a PCI compatible processor, however he discloses any generic processor complying with an I_2O specification can be used (col. 9, lines 33-38).

Odenwald teaches:

the input/output processor is a PCI-compatible processor (Fig. 2).

As per claim 12, Emerson discloses input/output adaptor being configured to be dynamically switchable between being controlled by the system processor and being controlled by the input/output processor (col. 8, lines 40-54).

Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

a method for optimizing processor utilization in a computer system having a system processor (Fig. 7, element 702), an input/output processor (Fig. 7, element 718), and an input/output adaptor (Fig. 7, element 720) connected to the system processor and the input/output processor (Fig. 7), the method for optimizing utilization comprising:

determining computer system utilization and switching control of the input/output adapter from a first one of the system processor and the input/output processor to a second one of the system processor and the input/output processor, if it is determined that the first one of the processors is being over utilized and that the second one of the processors has sufficient capacity that switching control of the input/output adapter will not adversely affect system throughput (col. 8, lines 2-15).

As per claim 13, Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

switching control of the input/output adapter from the first one of the processors to the second one of the processors is further based on a determination that the over utilization of the first of the processors is likely to continue for at least a specified period of time (col. 8, lines 2-15).

As per claim 14, Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

the steps of determining computer system utilization switching control of the input/output adapter based on such determination are repeated at intervals substantially equal to the specified period of time (col. 8, lines 2-15).

As per claim 15, Emerson fails to explicitly disclose a method for optimizing processor utilization.

Odenwald teaches:

the computer system has a plurality of dynamically switchable input/output adapters (Fig. 7), and the steps of determining computer system utilization switching control of the input/output adapter based on such determination are performed for each of the plurality of input/output adapters (col. 8, lines 2-15).

As per claim 19, Emerson discloses the input/output adapter; the input/output processor and the system processor are interconnected via a bus (Fig. 2).

Response to Arguments

Applicant's arguments filed January 30, 2007 have been fully considered but they are not persuasive.

As per claims 4 and 7, in response to applicant's argument that the Emerson reference fails to teach the limitations of "detecting a fault in the input/output processor;" and "switching the input/output adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected", Examiner respectfully disagrees.

Emerson's col. 8, lines 7-11 states upon system initialization, the slots/locations disposed on an I/O bus (for example, the slots located in front of the IOP) are defaulted to the Assigned condition (Fig. 4, element 402). The Assigned status indicates that the slot is assigned to an IOP and is controllable by it. Thus input/output adaptors are controlled by the input/output processor.

Emerson discloses the input/output adaptors would be controlled by the system processor (i.e. switching the input/output adapter to control by the system processor) if there is no suitable input/output processor executable driver module for the assigned adapter (col. 8, lines 40-43). Not finding a suitable input/output processor executable driver module is therefore lack of availability of the input/output processor, since driver module is executed by the input/output processor. This is an input/output processor fault condition and it is detected in (Fig. 4, element 414).

As per claims 8 and 11, in response to applicant's argument that the Emerson reference fails to teach the limitation of "detecting correction of the fault in the input/output processor; and switching the input/output adapter back to control by the input/output processor when the correction of the default is detected, if it was previously

switched to control by the system processor as a result of the fault in the input/output processor", Examiner respectfully disagrees.

Emerson discloses if an input/output processor DDM is detected to be present (i.e. available driver module that is executed by the input/output processor) the adapter is to be controlled by the input/output processor. Detection of the availability of a driver module is therefore detecting a correction of the fault (i.e. lack of availability) in the input/output processor (col. 8, lines 33-38).

As per claim 12, applicant argues that Odenwald neither teaches nor suggests switching control of an input/output adapter between an input/output processor and the system processor for the purpose of optimizing processor utilization. Examiner respectfully disagrees and notes that Odenwald's figure 2 shows a data processing system 200 includes a primary input/output platform (IOP) 208, which is connected to host 202 by primary bus 204. Additionally, IOP 208 is connected to secondary bus 206 and also functions as a PCI-to-PCI bus bridge. Data processing system 200 also includes adapter 212 and adapter 214. *Secondary IOPs 210 and 216 are intelligent adapters under I_2O and secondary IOP 210 and secondary IOP 216 contain input/output processors.* Adapters 212 and 214 are non-intelligent adapters, which do not contain input/output processors.

Odenwald's col. 9, lines 10-20 states placing intelligent adapters, which may be in the form of IOPs containing input/output processors, on a secondary bus that communicates with a primary IOP that is connected to a primary bus and the secondary bus. Functionality normally performed solely by IOPs on the secondary bus may be

placed also within the primary IOP to split up workloads and increase performance on the data processing system. Furthermore, communications between secondary IOPs and the primary IOP are set up such that the secondary IOPs see the primary IOP as the host processor (col. 9, lines 23-25).

As per claims 13-14, Odenwald's data processing system (Fig. 2, element 200) uses a standard architecture for intelligent input/output called the I_2O Specification, which defines an architecture that is independent of both the specific device being controlled and the host operating system. It defines an approach to input/output in which low level interrupts are offloaded from the CPU to I/O processors designed specifically to handle input/output. With support for message-passing between multiple independent processors, the I_2O architecture relieves the host of interrupt-intensive input/output tasks, greatly improving input/output performance (col. 4, lines 6-22).

Odenwald also discloses intelligent input/output real time operating system (IRTOS) which is a special purpose real time operating system designed to support high speed, low overhead input/output operations (col. 5, lines 35-45).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).